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FAULT-TOLERANT COMPUTING RESEARCH,  
INTERIM SCIENTIFIC REPORT, GRANT AFOSR-84-0052,  
15 JANUARY 1984 - 14 JANUARY 1985

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| 19. ABSTRACT (Continue on reverse if necessary and identify by block number)<br><p>This report provides a synopsis of research performed in fault-tolerant computing, for the first year of grant AFOSR-84-0052. Also included is a list of publications that have resulted from the research supported by this grant. Additionally, this report reviews the future direction for the continuing research under this grant.</p> <p>In the past year, this effort has focussed on the following problems:--- (1) Investigation of novel fault-tolerant processor array architectures with the potential of a high degree of defect tolerance, but having low processor and interconnect overhead associated with the fault tolerance mechanisms; (2) Development of realistic models to evaluate the yield, redundancy and performance tradeoffs for the designs. Such models would help establish the viability of these architectures, also enabling them to be compared with other designs in the literature; (3) Development of new and efficient testing strategies, and reconfiguration schemes for their structures; (4) Testable design of large size VLSI memory; and (CONTINUED)</p> |   |  |                      |                     |             |          |               |        |      |    |  |  |  |  |  |
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## I. INTRODUCTION

This report details those research accomplishments of the first year; AFOSR support, under grant 84-0052. Research focused primarily on the fault-tolerance aspects of large area VLSI circuits, particularly in the context of multiprocessor implementation of a single chip or wafer. Additional research was carried out in the area of the design of easily testable memory circuits, and the design of sorting networks on a single chip. The research performed has been recognized in the professional realm, evidenced by the list of accepted/published papers.

The report that follows is organized into three main sections. Section II summarizes the key research results obtained to date. Section III lists all of the papers and reports that have either already been accepted for publication, or that have been submitted for publication. Section IV closes the report by discussing future directions indicated for the continuing research.

## II. SUMMARY OF RESEARCH RESULTS

Last year's research focused on the following problems:

- 2.1 Investigation of novel fault-tolerant processor array architectures with the potential of a high degree of defect tolerance, but having low processor and interconnect overhead associated with the fault tolerance mechanisms.
- 2.2 Development of realistic models to evaluate the yield, redundancy and performance tradeoffs for our designs. Such models would help establish the viability of these architectures, also enabling them to be compared with other designs in the literature.
- 2.3 Development of new and efficient testing strategies, and reconfiguration schemes for our structures.
- 2.4 Testable design of large size VLSI memory.
- 2.5 Development of novel sorting networks that can be implemented on a single chip or wafer.

Highly parallel algorithms that solve many important computational problems have been known for several years. Regrettably, the large parallel processor arrays that are necessary to exploit the parallelism in these algorithms are expensive to implement; therefore, they have not been widely utilized. The proposed research has as its goal the development of design techniques that will allow such large high performance arrays to be implemented on a single large area wafer scale integrated circuit. This would make it feasible to use such processor arrays in relatively small, application-oriented systems; examples include on-board image analysis systems in remote vehicles, quick response robot control systems, etc.

As component sizes in VLSI approach the submicron level, increased chip complexity through smaller feature sizes appears more difficult to achieve. It is therefore clearly desirable to realize large area VLSI circuits. Unfortunately, any significant increase in chip area, including full wafer integration, remains an elusive goal primarily because of the large number

of fabrication defects which appear even in the best of VLSI manufacturing processes. It is clear that such large area VLSI circuits, in order to be viable, must be designed so as to be "defect tolerant"; i.e. they must operate correctly even in the presence of fabrication defects. However, traditional fault tolerant design approaches cannot be directly applied to this problem; also, the few defect tolerance schemes recently proposed in the literature are either limited in their applicability to memory circuits, or have other significant shortcomings.

Here, we address this important problem and these related issues: developing yield models for evaluating the effectiveness of the proposed fault tolerant designs; additionally, developing efficient testing strategies for these complex circuits.

Two specific topic areas which are related to such VLSI designs are the focus of our research; these are the areas of yield enhancement and performance improvement. Analytical models are being developed that evaluate how yield enhancement and performance improvement may both be achieved with the introduction of redundancy into the VLSI design.

Also developed is a taxonomy for fault-tolerant multiprocessor architectures on large area VLSI circuits. Such a taxonomy allows us to study strengths/weaknesses of various ad-hoc schemes that have been proposed. At the same time, we can develop new interconnect structures that utilize VLSI area more efficiently.

Also, we are carrying out the following research on system-level issues of fault-diagnosis in the context of multiprocessor implementation on a single chip or wafer.

Most previous research has considered either: (1) the diagnosability of a system with a predetermined static testing graph or (2) adaptive testing graphs (where one test is conducted at a time, its result determining the next test). Our approach is to determine a minimal testing graph (as measured by the number of edges) that may be applied to diagnose at least one fault. The distinction between our approach and earlier work is that the tests are neither conducted sequentially (as in adaptive methods) since the graph is known, nor is the graph static. Instead, after a fault has been diagnosed, a new minimal graph is used to diagnose subsequent faults.

We adopt a graph-theoretic model of a distributed computing system, where graph  $G = (V, E)$ . The vertices in  $V$  represent processors in the system; the edges in  $E$  represent communication links between processors. The edges in  $E$  are labelled  $(a, b)$ , where  $a$  and  $b$  are labels for vertices in  $V$ . Let there be  $n$  nodes in  $G$ ,  $n = |V|$ . The degree,  $d_i$ , of a node,  $i$ , is the number of nodes to which it is directly linked. The degree,  $d$ , of  $G$  is the maximum of  $d_i$  over all  $i$  in  $V$ . The distance between two nodes is the minimum number of edges that must be traversed to travel between them. The diameter,  $K$ , of  $G$  is the maximum of the distances between all possible pairs of nodes. The  $f$ -fault diameter,  $K_f$ , is the maximum of the diameters of all graphs obtainable from  $G$  by removing any  $f$  nodes. The connectivity,  $c$ , of  $G$  is the minimum number of nodes that must be removed in order to disconnect  $G$  ( $K_c = \infty$ ), or reduce it to a solitary node. ( $G$  can tolerate  $t = c-1$  faults without risking disconnection).

Thus, previous research derived the conditions determining precisely when a given set of tests in a homogeneous system achieved a specified level



of self-diagnosability. A new methodology is pursued here with the objective of minimizing the overhead associated with periodic testing.

Specifically, decreasing the testing required from  $O[nt]$  tests to  $O[n]$  tests would improve the performance of the system. The savings could be distributed in any way desired amongst these three factors:

(1) testing overhead. Some of the system time devoted to testing could be recovered for useful work.

(2) test reliability. The fewer tests could be allotted more time--likely making them more thorough.

(3) test frequency. The fewer tests could be conducted more frequently, yielding a better average time between component failure and detection.

Diagnosis must be considered in both synchronous and asynchronous environments. A synchronous environment is usually achieved by message passing; the processing elements operate as though with a common clock. A synchronous environment enjoys the advantage of allowing the processors to conduct their tests simultaneously. This feature permits diagnosis by an analysis of the set of test results.

In summary, we pursue a strategy of not utilizing the full capacity of the allowable testing graph in an effort to arrive at a more efficient diagnosis.

Also being investigated is a new design of easily testable memory. The impact of VLSI is no where more dramatic than in the area of Random Access Memory (RAM) design. The very marked improvement in RAM density has chiefly resulted from two factors: firstly, the improvement in fabrication technology has made way for a significant decrease in minimum feature size.

Secondly, the evolution of the storage cell within the RAM itself has seen a significant decrease in size - evolved from the initial 6 transistor static cell to the 1 transistor dynamic RAM cell.

Design improvements in the RAM have also brought on corresponding, significant problems, as described below.

### Testing Complexity

Dynamic single transistor cells permit very high integration densities and will probably be used in all future generations of memories. However, these cells are susceptible to charge leakage and alpha particle sensitivity. Charge leakage is a complex phenomenon and in general, is a function of the state of the neighboring cells, giving rise to pattern sensitivity. Also the proximity of the cells has given rise to crosstalk. These soft errors, together with the usual open, short and stuck-at faults, make memory testing a complex problem.

### Yield

Although this problem is not specific to memories, it is a major obstacle towards integrating larger memories on a chip. Since feature sizes will shrink more slowly, larger memories can only be obtained by increasing the die area and yield decreases exponentially with increasing area.

### Graceful Degradation

Memories have always been small, low-cost units; so until now, graceful degradation has not been an issue. However, as memory sizes move to the megabit range, each chip would represent a considerable percentage of the entire memory system. This would make the system very susceptible to single point failures. For example, if a one megabyte memory system is to be designed using 64K by 1bit chips, then the system would be organized as 16

banks of 8 chips each. If a single chip fails, then that bank can be isolated and the system can continue with reduced memory. If, however, 1M by 16 bit memory chips are used, then a single failure would cause the loss of the entire system. Even with the use of error correcting codes, the ability to degrade gracefully would warrant another layer of fault tolerance to the system. It is projected that this will be a requirement in future designs.

In order to address these just-described problems, a brand new RAM architecture is being developed here, with the following properties:

- (a) Provide redundancy at different levels to improve fault-tolerance and yield.
- (b) Provide easily testable properties that reduce the test complexity. The proposed design has the potential for keeping the testing time constant with the increase in the size of the RAM.
- (c) Provide graceful degradation for operational faults.

Already, significant progress to this end has been made and an actual prototype is being built, using the MOSIS facility. Finally, work is being carried out on de Bruijn multiprocessor networks. Specifically, we have derived results which use de Bruijn graphs to design a versatile sorting network.

Recent work has classified sorting architectures as, (A) Sequential input/Sequential output, (B) Parallel input/Sequential output, (C) Parallel input/Parallel output, (D) Sequential input/Parallel output and (E) Hybrid input/Hybrid output. The classification is based not only on the I/O method, but also on the sorting algorithm, as well as on the type of keys used. We have demonstrated that the architectures based on the undirected de Bruijn graphs (DGs) can sort data items in all of the above-mentioned categories. To the best of our knowledge, no other single network which can sort data items in all the categories is known. Sorting algorithms and time

complexities that correspond to each of these categories are derived here. These algorithms are distributed in the sense that these are executed by individual processors without any centralized controller. It is shown that these architectures can achieve the previously known best upper bound times, for all of the categories. Also, it is shown that they work as sorting networks, even in the presence of some faults.

## III. PUBLICATIONS SUPPORTED BY AFOSR 84-0052

Journals

1. "Synthesis of Directed Multicommodity Flow Networks," NETWORKS, Vol. 14, pp. 213-224 (with A. Itai).
2. "Fault-Tolerant Multiprocessor Link and Bus Network Architectures," IEEE Transactions on Computers, Vol. C-34, No. 1, Jan. 1985, pp. 33-46.
3. "Dynamically Restructurable Fault-tolerant Processor Network Architectures," IEEE Transactions on Computers, (to appear).

Reviewed Papers in Conference Proceedings

1. "A multiprocessor network suitable for single-chip VLSI implementation," Proceedings of the 11th Annual International Symposium on Computer Architecture, May 1984, pp. 328-337 (with M.R. Samatham).
2. "The De-Bruijn Multiprocessor Network: A Versatile Sorting Network," Proceedings of the 12th Annual International Symposium on Computer Architecture, June 1985 (to appear), (with M.R. Samatham).
3. "Fault-tolerant multi-bus architectures for multiprocessors," Proc. FTCS-14, Orlando, FL, June 1984, pp. 400-408 (with Z. Hanquan and M.L. Schlumberger).
4. "Dynamic Testing Strategy for Distributed Systems," Proc. FTCS-15, Ann Arbor, MI, June 1985 (with Fred Meyer).

#### IV. SYNOPSIS OF FUTURE RESEARCH

The goal of our research here is to develop area efficient and testable fault tolerant VLSI structures, and to investigate the feasibility and cost effectiveness of implementing them on a single large area (including wafer scale) integrated circuit. Towards this goal, we are undertaking the following research tasks.

4.1. We plan to develop new fault-tolerant architectures that will provide more efficient use of redundancy for yield and performance improvement. A broad class of existing networks will also be studied to determine techniques to incorporate fault-tolerance in these structures. We shall also develop a unified framework through which diverse fault-tolerance issues such as performance improvement and testability improvement can be studied.

4.2. Models for evaluating redundant VLSI structures will be developed. Our models will have wide applicability and will thus allow us to compare different designs. They will also be detailed enough to meaningfully predict fabrication yields. Furthermore, since it is useful to find methods by which one can optimally share available on-chip redundancy between yield enhancement and performance improvement, we also plan to develop such a model that can be used to study the effect of sharing available redundancy between these two somewhat competing requirements. No such models we believe yet exist.

4.3. Several problems related to testing and reconfiguration of these arrays will be studied. Our approach differs from the existing approaches

to multiprocessor diagnosis in that it is tailored specifically to the constraints posed by VLSI processor arrays. Both the distributed and centralized modes of testing will be considered.

4.4. To help establish the feasibility of some of the array structures, we will develop models that will allow realistic evaluation of their complexity. Also, we propose to layout and implement parts of proposed array structures using the VLSI CAD tools available at the university and the MOSIS facility. Some of the simpler array elements such as switch designs can be suggested as class projects in the two semester VLSI design course sequence, taught at the University.

4.5. Also, continuation of our research is planned into the area of the RAM design and the sorting networks.

The ultimate goal of our research is the full development of various aspects of fault-tolerant large area VLSI design.

## V. BIOGRAPHY AND VITA OF PRINCIPAL INVESTIGATOR

D.K. Pradhan

Dr. D.K. Pradhan is currently a Professor in the Department of Electrical and Computer Engineering, University of Massachusetts, Amherst. Previously he has held positions with Oakland University, Michigan and IBM Corporation, New York.

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████████████████████, received his M.S. from Brown University, Providence, Rhode Island in 1969 and Ph.D. from the University of Iowa, Iowa City, Iowa in 1972.

He has been actively involved with research in fault-tolerant computing and parallel processing since receiving his Ph.D. in 1972. He has presented several papers in fault-tolerant computing and parallel processing conferences. He has also published extensively in journals such as IEEE Transactions and Networks. His research interests include fault-tolerant computing, computer architecture, graph theory and flow networks.

Dr. Pradhan has edited the Special Issue on Fault-tolerant Computing, published in IEEE Computer, March 1980, served as Session Chairman and Program Committee member for various conferences. He is also an editor for the Journal of VLSI and Digital Systems and a Distinguished Visitor for IEEE Computer Society

Dr. Pradhan is also the editor of a forthcoming book entitled Fault-tolerant Computing: Theory and Techniques, to be published by Prentice Hall.



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| 9/78 - 12/82   | Associate Professor; School of Engineering, Oakland University, Rochester, Michigan.   |
| 9/73 - 7/78    | Associate Professor; Department of Computer Science; University of Regina; Regina, Canada.<br>(9/73-7/76 Assistant Professor). |

POSITIONS-VISITING

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| Summer 79 | Research Associate Professor; Stanford University; Computer Systems Lab.; Stanford, California.                             |
| Spring 78 | Visiting Associate Professor; Department of Electrical and Computer Engineering; Wayne State University; Detroit, Michigan. |

POSITIONS-INDUSTRIAL

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| 10/72 - 8/73   | Staff Engineer; (fault-tolerant group); IBM; Systems Development Lab.; Poughkeepsie, New York. |
| 1982 - present | Consultant to Mitre GTE and CDC in fault-tolerant computing.                                   |

EDUCATION

- 1972, Ph.D. (Electrical Engineering); University of Iowa; Iowa City, Iowa.  
Thesis area: Fault-Tolerant Computing
- 1970, M.S. (Electrical Engineering); Brown University; Providence, Rhode Island.  
Thesis area: Complexity Theory

PROFESSIONAL ACTIVITIES (HIGHLIGHTS)

- 1982 - 1985 IEEE Distinguished Visitor, Computer Society
- 1983 - 1984 Member, Program Committee, 11th Annual International Symposium on Computer Architecture.
- 1981 - Editor, Journal of VLSI and Digital Systems, Computer Science Press, Maryland.
- 1980 - 1981 Member, Program Committee, International Symposium on Fault-Tolerant Computing, June 81.
- 1979 - 1980 Guest Editor; Special Issue on Fault-Tolerant Computing; IEEE Computer, March 1980.
- 1980 Session Chairman, International Symposium on Fault-Tolerant Computing, Kyoto, Japan, October 1980.
- 1980 Session Chairman, International Symposium on Multivalued Logic, Evanston, Illinois, June 1980.
- 1980 Invited Paper, Fault-Tolerant VLSI Workshop, Los Angeles, California.
- 1978 Corresponding Member, International Symposium on Fault-Tolerant Computing; (France).
- 1977 Panelist; IEEE Compcon, (USA).
- 1976 Session Chairman; International Symposium on Multivalued Logic (USA).
- June 1975 Invited Lecturer; Gesellschaft für Mathematik und Datenverarbeitung; mbh Bonn; Bonn, West Germany.

## PUBLICATIONS

### TEXT BOOK

Fault-tolerant Computing: Theory and Techniques, (Ed) Prentice-Hall, Inc., (Forthcoming, July 1985).

### In Journals:

1. "Dynamically Restructurable Fault-tolerant Processor Network Architectures," (to appear) IEEE Transactions on Computers, 1985.
2. "Fault-tolerant Multilink Multibus Structures," IEEE Transactions on Computers, Vol. C-34, No. 1, January 1985.
3. "Synthesis of Directed Multi-Commodity Flow Problems," Networks, (with A. Itai) Vol. 14, 1984, pp. 213-224.
4. "Sequential Network Design Using Extra Inputs for Fault Detection," IEEE Transactions on Computers, Vol. C-32, No. 3, March, 1983.
5. "A Fault-Tolerant Distributed Processor Communication Architecture," IEEE Transactions on Computers, September, 1982, pp. 863-870 (with S. Reddy).
6. "A Class of Unidirectional Error Correcting Codes," IEEE Transactions on Computers, June, 1982, pp. 564-568 (with B. Bose).
7. "A Uniform Representation of Permutation Networks Used in Memory-Processor Interconnection," IEEE Transactions on Computers, Special Issue on Parallel Processing, September, 1980, (with K.L. Kodandapani), pp. 777-791.
8. "A New Class of Error Correcting-Detecting Codes for Fault-Tolerant Computer Applications," IEEE Transactions on Computers, Vol. C-29, No. 6, pp. 471-481, June, 1980.
9. "Error-Correcting Codes and Self-Checking Circuits," IEEE Computer, Vol. 13, Number 3, pp. 27-38, March, 1980 (with J.J. Stiffler).
10. "Undetectability of Bridging Faults and Validity of Stuck-at Fault Test Sets," IEEE Transactions on Computers, Vol. C-29, No. 1, (with K.L. Kodandapani) p. 55-59, January, 1980.
11. "Fault-Tolerant Asynchronous Networks Using Read-Only Memories," IEEE Transactions on Computers, Vol. C-27, No. 7, pp. 674-679, July, 1978.
12. "Fault Secure Asynchronous Networks," IEEE Transactions on Computers, Vol. C-27, No. 5, pp. 396-404, May, 1978.
13. "A Theory of Galois Switching Functions," IEEE Transactions on Computers, Vol. C-27, No. 3, pp. 239-249, March, 1978.

14. "Universal Test Sets for Multiple Fault Detection in AND-EXOR Arrays," IEEE Transactions on Computers, Vol. C-27, No. 2, pp. 181-187, February, 1978.
15. "Store Address Generator with Built-in Fault Detection Capabilities," IEEE Transactions on Computers, Vol. C-26, No. 11, pp. 1144-1147, November, 1977, (with M.Y. Hsiao & A.M. Patel).
16. "A Graph-Structural Approach for the Generalization of Data Management Systems," Information Sciences, American Elsevier Publishing Company, Inc., pp. 1-17, March, 1977.
17. "Techniques to Construct (2,1) Separating Systems from Linear Codes," IEEE Transactions on Computers, (with S.M. Reddy), Vol. C-25, No. 9, pp. 945-949, September, 1976.
18. "Reed-Muller Canonic Forms for Multivalued Functions," IEEE Transactions on Computers, (with A.M. Patel), Vol. C-24, No. 2, pp. 206-220, February, 1975.
19. "Fault-Tolerant Carry Save Adders," IEEE Transactions on Computers, Vol. C-23, No. 11, pp. 1320-1322.
20. "Design of Two-Level Fault-Tolerant Networks," IEEE Transactions on Computers, Vol. C-23, No. 1, pp. 41-48, (with S.M. Reddy), June, 1974.
21. "Fault-Tolerant Asynchronous Networks," IEEE Transactions on Computers, Vol. C-22, No. 7, pp. 662-669, July, 1973 (with S.M. Reddy),
22. "Error Control Techniques for Logic Processors," IEEE Transactions on Computers, Vol. C-21, No. 7, pp. 1331-1337 (with S.M. Reddy), December, 1972.

#### In Conference Proceedings

23. "Fault-tolerant Multibus Architectures for Multiprocessors," Proc. FTCS-14, June 1984, Kissimee, Florida, (with M.L. Schlumberger and Z. Hanquan) pp. 400-408.
24. "A Multiprocessor Network Suitable for Single Chip VLSI Implementation," Proc. 1984 IEEE 11th Annual Int. Symp. on Computer Architecture, June 1984, pp. 328-337.
25. "Fault-Tolerant Network Architectures for Multiprocessors and VLSI Based Systems," Proc. FTCS-13, Milan, Italy, June, 1983.
26. "On a Class of Multiprocessor Network Architectures," Proc. of International Conference on Distributed Processing, Miami, Florida, October, 1982, pp. 302-311, (Also reprinted in Interconnection Networks for Parallel and Distributed Processing edited by C. Wu and T. Feng, Aug. 1984).

27. "Interconnections Topologies for Fault-Tolerant Parallel and Distributed Architectures," Proc. of 10th International Conference on Parallel Processing, pp. 238-242, August, 1981.
28. "Testing for Delay Faults in a PLA," Proc. International Conference on Circuits and Computers, (with K. Son) September 1982, pp. 346-349.
29. "Fault-Diagnosis of Parallel Processor Interconnection Networks," Proc. Eleventh Annual International Symposium on Fault-Tolerant Computing, pp. 209-212, June, 1981 (with K.M. Falavarajani).
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